CLAIMS

1. An advanced telecommunications processor, comprising:

a plurality of multithreaded processor cores each having a data cache and instruction cache;

a data switch interconnect coupled to each of the processor cores and configured to pass information among the processor cores; and

a messaging network coupled to each of the processor cores and a plurality of communication ports.

2. The advanced telecommunications processor of claim 1, further comprising:

the data switch interconnect is coupled to each of the processor cores by its respective data cache; and

the messaging network is coupled to each of the processor cores by its respective instruction cache.

3. The advanced telecommunications processor of claim 1, further comprising:

a level 2 cache coupled to the data switch interconnect and configured to store information accessible to the processor cores.

4. The advanced telecommunications processor of claim 2, further comprising:

a level 2 cache coupled to the data switch interconnect and configured to store information accessible to the processor cores.

5. The advanced telecommunications processor of claim 1, further comprising:

an interface switch interconnect coupled to the messaging network and the plurality of communication ports and configured to pass information among the messaging network and the communication ports.

6. The advanced telecommunications processor of claim 2, further comprising:

an interface switch interconnect coupled to the messaging network and the plurality of communication ports and configured to pass information among the messaging network and the communication ports.

7. The advanced telecommunications processor of claim 3, further comprising:

an interface switch interconnect coupled to the messaging network and the plurality of communication ports and configured to pass information among the messaging network and the communication ports.

8. The advanced telecommunications processor of claim 4, further comprising:

an interface switch interconnect coupled to the messaging network and the plurality of communication ports and configured to pass information among the messaging network and the communication ports.

9. The advanced telecommunications processor of claim 1, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

10. The advanced telecommunications processor of claim 2, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

11. The advanced telecommunications processor of claim 3, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

12. The advanced telecommunications processor of claim 4, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

13. The advanced telecommunications processor of claim 5, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

14. The advanced telecommunications processor of claim 6, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

15. The advanced telecommunications processor of claim 7, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

16. The advanced telecommunications processor of claim 8, further comprising:

a memory bridge coupled to the data switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect and the communication port.

17. The advanced telecommunications processor of claim 1, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

18. The advanced telecommunications processor of claim 2, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

19. The advanced telecommunications processor of claim 3, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

20. The advanced telecommunications processor of claim 4, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

21. The advanced telecommunications processor of claim 5, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

22. The advanced telecommunications processor of claim 6, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

23. The advanced telecommunications processor of claim 7, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

24. The advanced telecommunications processor of claim 8, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

25. The advanced telecommunications processor of claim 9, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

26. The advanced telecommunications processor of claim 10, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

27. The advanced telecommunications processor of claim 11, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

28. The advanced telecommunications processor of claim 12, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

29. The advanced telecommunications processor of claim 13, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

30. The advanced telecommunications processor of claim 14, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

31. The advanced telecommunications processor of claim 15, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.

32. The advanced telecommunications processor of claim 16, further comprising:

a super memory bridge coupled to the data switch interconnect, the interface switch interconnect and at least one communication port, and configured to communicate with the data switch interconnect, the interface switch interconnect and the communication port.